Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Canceled)

2. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein the speed-increasing circuit includes a PMOS transistor.

3. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second-long distance wiring.

4. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.

5. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver

circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein a plurality of speed-increasing circuits are additionally inserted between an intermediate position of the second long-distance wiring and the vicinity of the input terminal of the gate circuit connected to a position corresponding to that intermediate position.

6. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein a plurality of buffer circuits are inserted at the input side of the second long-distance wiring.

7. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver

circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein a buffer circuit is inserted at the input side of the second long-distance wiring, and a buffer circuit is inserted at the output side of the second long-distance wiring.

8. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein the input signal (VIN) is realized by a word line selecting signal; the driver circuit is realized by a word line driver; the first long-distance wiring is realized by a word line (WL); and the gate circuits are realized by memory cells.

9. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in Claim 1,~~ comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit located furthest away on the first long-distance wiring from an output of the driver circuit and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, and

wherein the input signal (VIN) is realized by a clock input signal (VCK); the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.

10. (Previously Presented) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second long-distance wiring.

11. (Previously Presented) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.

12. (Previously Presented) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a plurality of speed-increasing circuits are additionally inserted between an intermediate position of the second long-distance wiring and the vicinity of the input terminal of the gate circuit connected to a position corresponding to the intermediate position.

13. (Previously Presented) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a plurality of buffer circuits are inserted at the input side of the second long-distance wiring.

14. (Previously Presented) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a buffer circuit is inserted at the input side of the second long-distance wiring, and a buffer circuit is inserted at the output side of the second long-distance wiring.

15. (Previously Presented) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the

driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the input signal (VIN) is realized by a clock input signal (VCK); the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.

Claim 16. (Canceled)

17. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein the speed-increasing circuit includes a PMOS transistor.

18. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second wiring.

19. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.

20. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein a plurality of speed-increasing circuits are additionally inserted between an intermediate position of the second wiring and the vicinity of the input

terminal of the gate circuit connected to a position corresponding to the intermediate position.

21. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein a plurality of buffer circuits are inserted at the input side of the second wiring.

22. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein a buffer circuit is inserted at the input side of the second wiring.

23. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein the input signal is realized by a word line selecting signal; the driver circuit is realized by a word line driver; the first wiring is realized by a word line; and the gate circuits are realized by memory cells.

24. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~as claimed in claim 16,~~ comprising a driver circuit, a first wiring coupled to the driver circuit, a plurality of gate circuits coupled over an entire length of the first wiring so that an input signal is received by the plurality of gate circuits via the driver circuit and the first wiring, and a second wiring and a speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring, and

wherein the input signal is realized by a clock input signal; the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.

Claims 25-27. (Canceled)